Hereinafter, a manufacturing method of a thin-film transistor array panel according to an exemplary embodiment of the present invention will be described with reference to accompanying drawings.

FIG. **3** is a layout view of a thin-film transistor array panel according to exemplary embodiments. FIG. **4** is a cross-sectional view taken along lines IV-IV' and IV'-IV" of FIG. **3**. FIG. **5** is a layout view of a next step of FIG. **3**. FIG. **6** is a cross-sectional view taken along lines VI-VI' and VI'-VI" of FIG. **5**. FIG. **7** is a layout view of a next step of FIG. **5**. FIG. **8** is a cross-sectional view taken along lines VIII-VIII' and VIII'-VIII" of FIG. **7**. FIG. **9** is a layout view of a next step of FIG. **7**. FIG. **10** is a cross-sectional view taken along lines X-X' and X'-X" of FIG. **9**.

Referring to FIG. **3** and FIG. **4**, a gate line **121** having a first gate electrode **125** and a gate pad **129** is formed on a substrate **100**.

A self-assembled monolayer **35** and **39** is respectively formed on the gate line **121**, by coating an electron acceptor material or an electron donor material, to form a preliminary monolayer. The preliminary monolayer may be a polymer material including the thiol group having large affinity with the metal. The preliminary monolayer may be formed by a spin coating, a dip coating, or a vaporization method. When using the spin coating, the thickness of the preliminary monolayer may be controlled by controlling a concentration of a coated solution.

Next, the preliminary monolayer not reacted with the gate line **121** is removed through cleansing, to form the first self-assembled monolayer **35** and **39**, such that the first self-assembled monolayer **35** and **39** is formed only on a portion of the gate line **121** corresponding to the first gate electrode **125** and the gate pad **129**.

Next, referring to FIG. **5** and FIG. **6**, a gate insulating layer **140** is formed on the substrate **100**, and a semiconductor **154** overlapping the first gate electrode **125** is formed on the gate insulating layer **140**. The semiconductor **154** may be formed of an oxide semiconductor.

Next, referring to FIG. **7** and FIG. **8**, an etching stop layer **150** is formed on the substrate **100**, and the etching stop layer **150** is selectively etched to form contact holes **81** and **83** exposing the semiconductor **154**, and a contact hole **69** exposing the gate pad **129**. According to an exemplary embodiment of the present invention, the etching stop layer **150** may be formed only on the channel of the semiconductor **154** without the contact hole.

Next, referring to FIG. **9** and FIG. **10**, a metal layer is formed on the etching stop layer **150**. The metal layer is patterned to form a source electrode **173** and a drain electrode **175** connected to the semiconductor **154** through the contact holes **81** and **83**, and an assistance gate pad **77** connected to the gate pad **129** through the contact hole **69**. The etching stop layer **150** may cover the channel of the semiconductor **154** to protect the channel, thereby preventing the channel of the semiconductor **154** from being exposed and damaged.

Next, a first interlayer insulating layer **160** is formed on the substrate **100**, and a preliminary monolayer including the electron donator material or the electron acceptor material is formed on the first interlayer insulating layer **160**. The preliminary monolayer may be formed of polymer material including a silane group, which may react with the first interlayer insulating layer **160**.

Next, a metal layer is formed on the preliminary monolayer and patterned to form the second gate electrode **127**. The preliminary monolayer is removed by using the second gate electrode **127** as a mask, to complete a second self-assembled monolayer **37** positioned between the second gate electrode **127** and the first interlayer insulating layer **160**.

Next, referring back to FIG. **1** and FIG. **2**, a second interlayer insulating layer **180** is formed on the substrate **100**. Subsequently, a metal layer is formed on the second interlayer insulating layer **180** and patterned to form a pixel electrode **191** and contact assistants **97** and **99**.

Although certain exemplary embodiments and implementations have been described herein, other embodiments and modifications will be apparent from this description. Accordingly, the inventive concept is not limited to such exemplary embodiments, but rather to the broader scope of the presented claims and various obvious modifications and equivalent arrangements.

What is claimed is:

1. A thin-film transistor array panel, comprising:
- a substrate;
- a first gate electrode disposed on the substrate;
- a first self-assembled monolayer disposed on the first gate electrode;
- a gate insulating layer disposed on the first self-assembled monolayer;
- a semiconductor disposed on the gate insulating layer;
- a drain electrode overlapping the semiconductor, the drain electrode being separated from and facing a source electrode with respect to the semiconductor;
- a first interlayer insulating layer disposed on the source electrode and the drain electrode;
- a second self-assembled monolayer disposed on the first interlayer insulating layer;
- a second gate electrode disposed on the second self-assembled monolayer;
- a second interlayer insulating layer disposed on the second gate electrode; and
- a pixel electrode disposed on the second interlayer insulating layer and connected to the drain electrode.

2. The thin-film transistor array panel of claim **1**, wherein:
- the first gate electrode is configured to receive a scan signal from a gate line disposed on the substrate; and
- the second gate electrode is configured to be floated.

3. The thin-film transistor array panel of claim **1**, wherein:
- the first self-assembled monolayer comprises a first polymer material comprising a thiol group; and
- the second self-assembled monolayer comprises a second polymer material comprising a silane group.

4. The thin-film transistor array panel of claim **3**, wherein:
- the first self-assembled monolayer comprises a fluoroaryl thiol derivative; and
- the second self-assembled monolayer comprises a fluoroaryl silane derivative or a fluoroalkyl silane derivative.

5. The thin-film transistor array panel of claim **4**, wherein the semiconductor is an N-type semiconductor.

6. The thin-film transistor array panel of claim **3**, wherein:
- the first self-assembled monolayer comprises an aminoaryl thiol derivative; and
- the second self-assembled monolayer comprises an aminoalkyl silane derivative or an aminoaryl silane derivative.

7. The thin-film transistor array panel of claim **6**, wherein the semiconductor is a P-type semiconductor.

8. The thin-film transistor array panel of claim **1**, wherein:
- the first self-assembled monolayer is disposed between the gate insulating layer and the first gate electrode; and
- the second self-assembled monolayer is disposed between the first interlayer insulating layer and the second gate electrode.